

ABSTRACT OF THE DISCLOSURE

In a shift register block according to the present invention, a plurality of flip-flops $F/F(1)$, $F/F(2)$, ... $F/F(n)$ constitute a shift register SR, and each adjacent ones of these flip-flops are therebetween having a corresponding one of waveform processing circuits $WR(1)$ through $WR(n)$, so that the shift register SR and the waveform processing circuits $WR(1)$ and $WR(n)$ are linearly aligned. With such an arrangement, it is possible to reduce area occupied by a signal line driving circuit including the shift ~~sift~~ register block, thereby narrowing the frame area of a display device.